Chapter 12

Lab 1

Introduction to a basic dc-to-dc power conversion system and the PECS circuit simulator

12.1 Objectives

1. To introduce a basic dc-to-dc power conversion system.
2. To introduce the PECS simulator which simulates these systems at the circuit level. Specifically to gain experience with the use of the *switch* (SW), *pulse width modulator* (MOD) and *clock* (CLK) elements used in PECS and which appear in later labs.

Before using the PECS simulator, read the documentation which provides an overview of PECS sufficient for this and subsequent labs.

12.2 Circuit #1

The circuit in Figure 12.1 switches a voltage source (V1) ON and OFF to produce a rectangular wave (appearing across voltage port VP1) which is then filtered through an LC network which produces a lower dc voltage across a load (R1). This voltage, monitored by port VP2, will be examined.

This example circuit also illustrates how *clock* elements can be used to control switches.

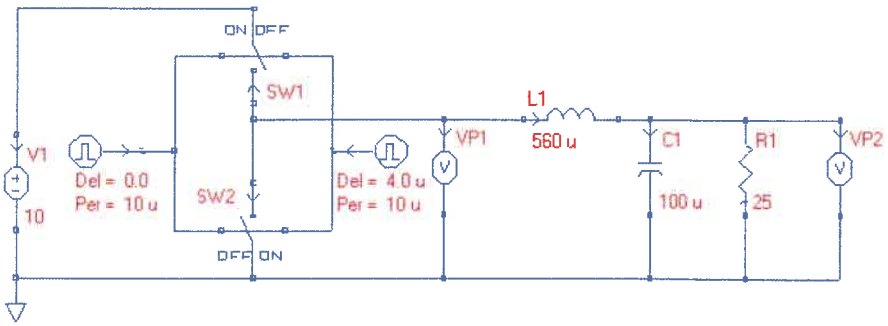

Figure 12.1: A pulse generator followed by a second order (LC) filter, ($L = 560\ \mu H$, $C = 100\ \mu F$ and $R = 25\ \Omega$) constitutes a dc-to-dc voltage converter. (buck_clocks.ckt)

12.2.1 Tasks

1. Construct the circuit in Figure 12.1 in PECS. Leave the initial conditions for L and C at zero and set the initial state of the switches to ON and OFF for the top and bottom switches, respectively. (However, the initial switch state is not important here but must be set to some state prior to trying to run a simulation). Also, be aware when building the circuit that connections to components are only made at the nodes of the components

2. Use the following simulation parameters: *Final Time* = 6e-2, *Step Size* = 2e-7, *Start time* = 0, *End time* = 6e-2. These simulation parameters will provide a simulation of the circuit for 60 *ms* (as specified by *Final Time*) where recording of the waveform points occur every 200 *ns* (as specified by *Step Size*) as well as points occurring at switching discontinuities. At the end of the simulation time points occurring between the *Start Time* and *End Time* will be saved to the hard drive, which will subsequently be read by the plotting program (PECSPLOT). For the times chosen here, points from the whole simulation run will be saved. The relatively short *Step Size* value chosen results in many points being saved which will produce smooth output plots.

3. Run the simulation. This can be initiated from the menu items by selecting *Simulation* → *Run*, or more conveniently from the top icon bar by clicking the (left) script R (which appears in red).

4. Obtain a plot of the waveform across VP2, the output voltage. Looking at your plot determine the steady state value, that is, the value of the output voltage at the end of the simulation.

5. We would like to now look more closely at 4 or 5 cycles at the end of the simulation. Use the *Zoom* feature in PECSPLOT to isolate these. Access

this through menu items *View* → *Zoom* and then use the mouse to isolate the time period of interest. Left click the mouse anywhere in the plotting area at the desired starting time and drag to the desired ending time. This can be repeated any number of times to hone into your desired time interval.

6. Under the plot obtained in the previous task add the VP1 waveform. Do this by accessing from the menu items: *Plots* → *Add Plot* then select the desired out from the list of outputs shown.

7. Use the measuring feature (accessed through menu item *Plots* → *Measure*) to find the peak-to-peak voltage ripple of the output voltage (VP2). Use the right (→) and left (←) arrows on the keyboard to precisely pinpoint the maximum and minimum values of the waveform after initially placing the measurement markers by clicking the left and right mouse buttons.

8. For the waveform of VP1, note the peak amplitude, period and pulse width of this waveform. Determine the *duty ratio* of the pulse train. The duty ratio is defined as the length of the high portion of the pulse, i.e. the pulse width, divided by the period.

9. Taking the above plots into consideration, explain why you would expect to get the steady state value you found in task (4).

12.3 Circuit #2

The circuit in Figure 12.2 produces a sawtooth voltage waveform which appears across the capacitor (C1). This is achieved by using a constant current source (I1) to charge the capacitor and having the capacitor rapidly discharged through the resistor (R1) when the voltage has reached a preset level. The capacitor voltage and current are monitored by VP1 and IP1, respectively.

This circuit illustrates the use of the pulse width modulator element. However, in this circuit not all features of the modulator are used. The modulator is basically a comparator with four inputs, two of which connect externally, one connects to a user set constant value and the last connects to an internal sawtooth signal. We will just use one of the external connections and the internal constant input. (The internal sawtooth signal is not used).

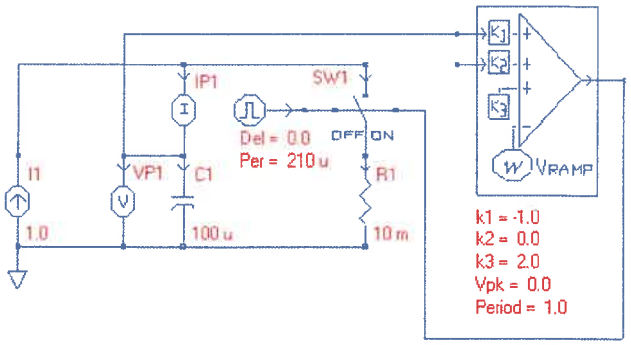

Figure 12.2: Sawtooth generator. A 1 A current source charges a 100 μF capacitor which is periodically quickly discharged through a 10 mΩ resistor. (sawtooth_3.ckt)

12.3.1 Tasks

1. Construct the circuit in Figure 12.2 in PECS. Note that for the modulator we are setting $K_1 = -1$ and $K_3 = 2$, with the other modulator parameters left untouched. The clock element has a *Delay* = 0 and *Period* = 210e-6.

2. Use the following simulation parameters: *Final Time* = 1e-3, *Step Size* = 1e-6, *Start time* = 0, *End time* = 1e-3. Run the simulation.

3. Obtain a plot of the voltage waveform across the capacitor (VP1) and under this have a plot of the capacitor current (IP1).

4. For the waveform of VP1, note the peak amplitude and period. Given that $K_1 = -1$, what other factors in the circuit determines the peak amplitude and why?

12.4 Circuit #3

We will modify the circuit in Figure 12.1 by replacing one of the clocks with a modulator and a DC voltage source. The modulator output is connected to the switch control terminal where the deleted clock had been. The added voltage source's positive terminal is connected to the top input of the modulator. The negative terminal is connected to ground. The configuration we are seeking is for the modulator to turn OFF the upper switch (and turn ON the lower switch).

The modulator parameter K_1 associated with the top modulator input is set to $K_1 = 1$. (Also be sure to have $K_2 = 0$ and $K_3 = 0$). We will also specify the modulator internal sawtooth to have a peak voltage of 5 V, i.e. $V_{pk} = 5$.

Furthermore, we will change the frequency of operation of this circuit to 40 kHz. So the period parameters of the modulator and the remaining clock should be changed to 25 μs, i.e. set $Period = 25\ \mu s$, for both these components.

Also, we will operate the circuit at 50% duty ratio. Determine the value of the voltage source needed to achieve this, given the parameters stated above.

12.4.1 Tasks

1. Obtain a copy of your schematic. (buck_mod.ckt)
2. Repeat the tasks of Circuit #1.
3. Complete the following table.

	Switching Frequency	Duty Ratio	Peak-to-peak Input Voltage to Filter	Steady State Average Output Voltage	Peak-to-peak Output Voltage Ripple
Circuit #1					
Circuit #3					

4. Explain the differences seen in the peak-to-peak ripple voltage values between Circuit #3 and Circuit #1. Are they in line with your expectations? Why?